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A Systems Approach to Large-Scale Molecular and Nanoelectronic Memory & Logic Circuits

Abstract—If the projections from the International Technology Roadmap for Semiconductors (ITRS) hold, then by the year 2020 it is expected that the most closely spaced metallic wires within a DRAM circuit will be patterned at a pitch of about 30 nm, implying that the conductors themselves will be of a width of around 15 nm. However, virtually every aspect of achieving this technology is considered to be 'red,' meaning that there is no known solution. Several years ago we began working on developing the architectures, devices, molecules, circuitry, and manufacturing processes for testing the limits of how far electronics circuitry could be scaled, with the basic presumption that any solution would require a combination of passive and active molecular components, semiconductor and metallic nanowires, and defect-tolerant architectures and manufacturing. In this talk, I will present results in which we have constructed large scale circuitry (> 10^5 devices) at densities that span the ITRS projections between the years 2020 and 2030. This will include a 160,000 bit memory circuit that is no larger than a white blood cell, demultiplexing circuits for such memories, and high-performance, ultra-dense logic circuitry that is energy efficient, exhibits gain, and constitutes a complete logic set. I will also discuss the molecular components and how we have learned, through thermodynamic and kinetic measurements of their switching processes, to optimize their performance within these extreme settings.